A Passive Soft-Switching Snubber for PWM Inverters*

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***Abstract* — This paper presents a regenerative passive snubber circuit for PWM inverters to achieve soft-switching purposes without significant cost and reliability penalties. This passive soft-switching snubber (PSSS) employs a diode/capacitor snubber circuit for each switching device in an inverter to provide low dv/dt and low switching losses to the device. The PSSS further uses a transformer-based energy regenerative circuit to recover the energy captured in the snubber capacitors. All components in the PSSS circuit are passive, thus leading to reliable and low-cost advantages over those soft-switching schemes relying on additional active switches. The snubber has been incorporated into a 150 kVA PWM inverter. Simulation and experimental results are given to demonstrate the validity and features of the snubber circuit.**

I. Introduction

To reduce switching stresses, losses, and electromagnetic interference (EMI), soft-switching techniques have been developed for power converters since the 1970s [1]. There are many topologies of soft-switching inverters [1–10], such as resonant dc link, resonant snubber, and zero-current transition inverters [8]. Soft-switching inverters can be grouped into two main categories: resonant dc link and resonant snubber. The resonant dc link provides zero dc-link voltage or current intervals to all phase legs during switching instants, whereas the resonant snubber diverts current from and/or provides zero-voltage intervals to each main device at switching instants. The active clamped resonant dc link converter [1] and the auxiliary quasi-resonant dc link converter [2, 10] are examples of the resonant dc link inverters. Auxiliary resonant snubber inverters such as the auxiliary resonant commutated pole (ARCP), zero-voltage transition, and resonant snubber inverters [9] belong to the second resonant snubber category.

However, all existing soft-switching inverters use additional active devices to achieve soft-switching, thus increasing costs and control complexity and decreasing reliability. Prior to the soft-switching technology, the RCD snubber circuit that consists of a resistor (R), capacitor (C), and diode (D), as shown in Fig. 1, had been widely used in PWM inverters to reduce switching stresses and EMI. The traditional RCD snubber is lossy and bulky, and is difficult to apply to high-frequency switching PWM inverters because the losses in the snubber increase proportionally with the switching frequency.

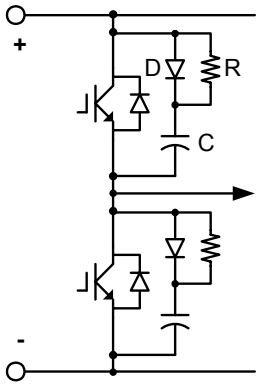

Fig. 1. An inverter phase leg with RCD snubbers.

This paper presents a regenerative passive snubber circuit for PWM inverters that is able to achieve the aforementioned soft-switching objectives without significantly increasing the cost. This passive soft-switching snubber (PSSS) employs a snubber circuit consisting of diodes and capacitors for each phase leg to provide low dv/dt and low switching losses to the switching devices. The PSSS further uses a transformer-based energy regenerative circuit to recover the energy captured in the snubber capacitors. All components in the PSSS circuit are passive, making it reliable and low in cost. The snubber has been applied to a 150 kVA PWM inverter. Simulation and experimental results are given to demonstrate the validity and features of the snubber circuit.

II. PSSS Circuit and Operating Principle

Fig. 2(a) shows the proposed PSSS circuit, which consists of a diode/capacitor soft-switching snubber (SSS) circuit for each phase leg, and an energy recovery circuit shared among all the phase legs, as illustrated in Fig. 2(b) for a three-phase inverter application. The SSS circuit includes a snubber diode, D_{Sp}, and a snubber capacitor, C_{Sp}, for the upper main device, S_p, and, symmetrically, D_{Sn} and C_{Sn} for the lower main device, S_n. The functions of the

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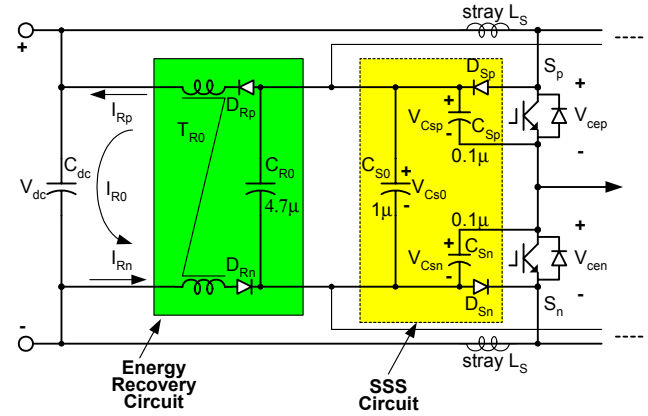
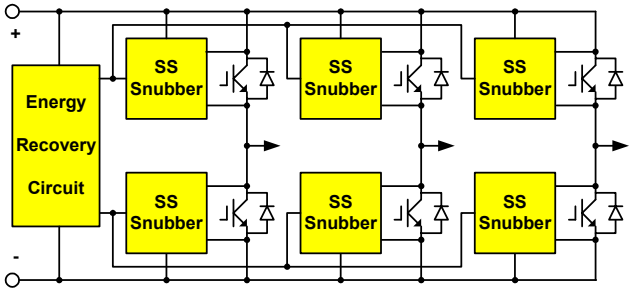
snubber diodes, D_{Sp} and D_{Sn}, and snubber capacitors, C_{Sp} and C_{Sn}, are very similar to those of the traditional RCD snubber. They are, however, arranged differently so that both snubber capacitors are connected to the midpoint of the phase leg. Since the upper and lower main devices always operate complementarily to each other during normal PWM operation, the sum of both snubber capacitors' voltages should remain constant and equal to the dc link voltage, which is further guaranteed by a larger snubber bus capacitor, C_{S0}, connected across the two snubber capacitors.



(a) Proposed PSSS circuit for an inverter phase leg



(b) Arrangement of a three-phase inverter with the PSSS circuits

Fig. 2. PSSS circuit for an inverter phase leg.

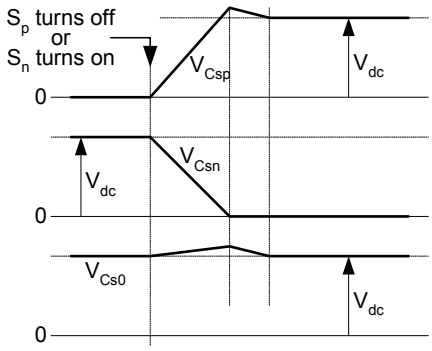


Fig. 3. Voltage waveforms at a switching instant showing the operating principle.

Fig. 3 shows the operating waveforms during S_p turn-off or S_n turn-on. Assuming the IGBT of S_p is conducting the load current, turning off S_p will divert the current into the snubber circuit, charging the snubber capacitor C_{Sp} through the snubber diode D_{Sp} and discharging C_{Sn} through C_{S0}. Therefore, V_{CSp} increases and V_{CSn} decreases as shown in Fig. 3, whereas voltage, V_{Cs0}, remains almost constant.

The energy recovery circuit that is shared by all the snubber circuits includes a capacitor, C_{R0}, two diodes, D_{Rp} and D_{Rn}, and a transformer, T_{R0}. The transformer, T_{R0}, makes I_{Rp} equal to I_{Rn} so that a recovery current, I_{R0}, flows into the dc link capacitor, C_{dc}. The two diodes, D_{Rp} and D_{Rn}, guarantee the energy recovery current (power) flows in one direction, i.e., from the snubber back to the dc link. The power (or current) rating of the energy recovery circuit for a three-phase inverter, P_R, is determined by the snubber capacitance, C_S (= C_{Sp} = C_{Sn}); dc link voltage, V_{dc}; inverter switching frequency, f_{sw}; stray inductance, L_s; square of the decrease in the dc link current over each switching instance, $\Delta I^2_{dc(k)}$; and fundamental frequency, f_m, according to the following equation.

$$P_R = 6C_S V^2_{Cs0} f_{sw} + f_m L_s \sum_k (\Delta I^2_{dc(k)}) \qquad (1)$$

A detailed analysis of the circuit can be performed based on operation modes given in Fig. 4. To simplify the analysis, as shown in the equivalent circuit in Fig. 4(a), the energy recovery circuit is omitted; it will be discussed later. The switching process from an upper switch carrying the load current to the lower diode is first described, and the process from an upper diode conducting the load current to the lower switch is then explained. Operation modes in the reversal of the two processes can be analogously derived.

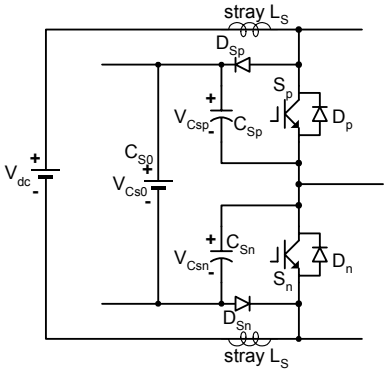
Mode 0+, Fig. 4(b): An initial mode in which switch S_p is conducting the load current, i_L. An inductive load is considered, and the load current remains constant during the switching process.

Mode 1, Fig. 4(c): S_p is turned off. The load current is diverted to the snubber capacitors, C_{Sp} and C_{Sn} through the snubber diode, D_{Sp}. The current thus charges C_{Sp} and discharges C_{Sn}.

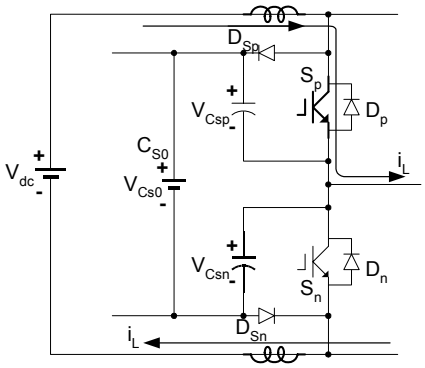
Mode 2, Fig. 4(d): When the voltage of C_{Sp}, V_{Csp}, increases to the dc source voltage, V_{Cs0}, and the voltage of C_{Sn}, V_{Csn} decreases to zero, the diodes, D_{Sn} and D_n start conducting, clamping V_{Csn} to zero. The current following the stray inductance is also decreasing.

Mode 3, Fig. 4(e): The current following the stray inductance decreases to zero, and the energy stored in the stray inductance is transferred to the snubber capacitor. The diode, D_n, carries the load current. Switch S_n can be turned on under zero voltage. During this mode, as the voltage across the capacitor, C_{S0}, becomes higher than the dc source voltage, the energy recovery circuit starts to transfer energy from the capacitor back to the dc source.

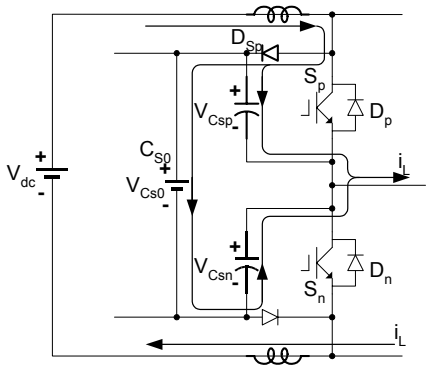
Mode 4, Fig. 4(f): Switch S_n is turned on in Mode 1 before C_{Sp} is fully charged and C_{Sn} discharged. Besides the load current, an additional charging/discharging current is generated through S_n, accelerating the charging/discharging process. At the end of the process, if the current following through C_{Sp} is bigger than the load current, the operation of the circuit proceeds to Mode 5. Otherwise, it falls back to Mode 2.



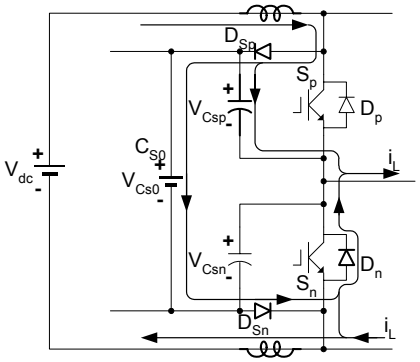
(a) Equivalent circuit of the snubber circuit during switching.



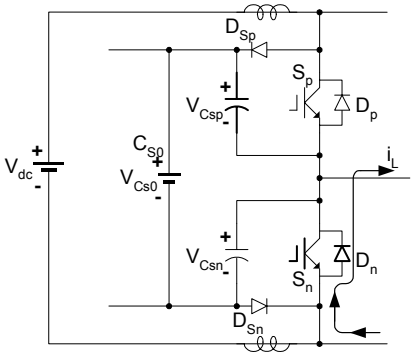
(b) Mode 0+: S_p is on and conducting load current.



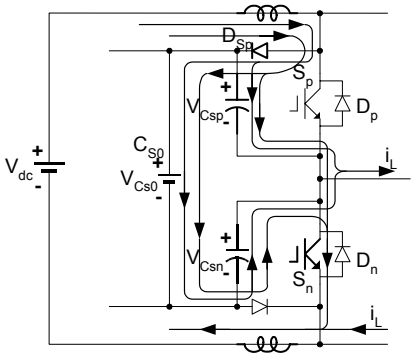
(c) Mode 1: S_p is turned off, charging C_{sp} and discharging C_{sn}.



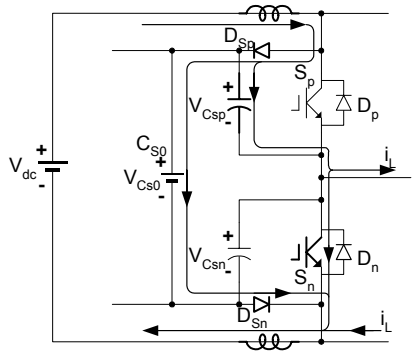
(d) Mode 2: D_{Sn} and D_n clamp V_{Csn} to zero voltage and carry current.



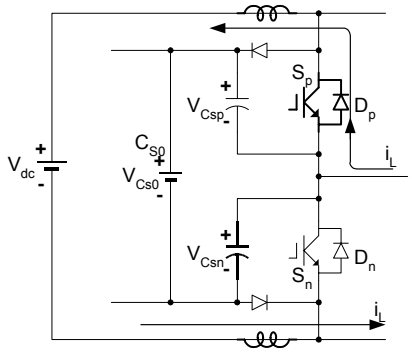
(e) Mode 3: D_n carries the load current and S_n is turned on.



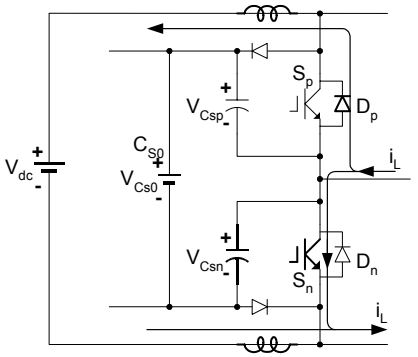
(f) Mode 4: S_n is turned on in Mode 1 before C_{sp} is fully charged and C_{sn} fully discharged. Turning on S_n accelerates the charge (C_{sp}) and discharge (C_{sn}) process.



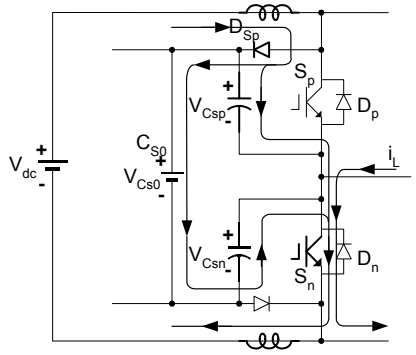
(g) Mode 5: C_{sn} is fully discharged. S_n carries a portion of the charging current.



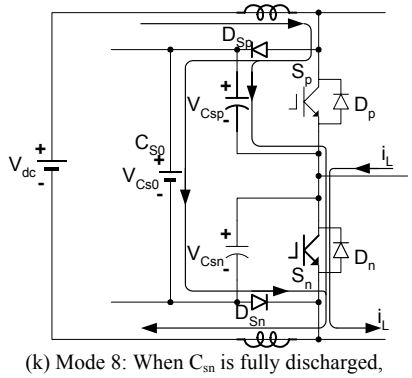
(h) Mode 0-: S_p is on while D_p is conducting the load current.



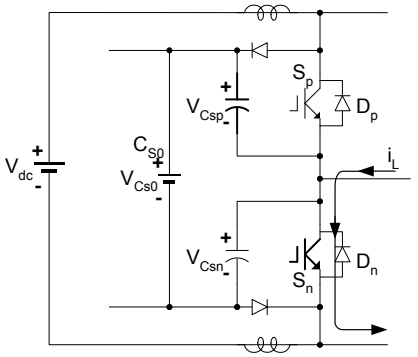
(i) Mode 6: S_n is turned on; thus a portion of the load current is diverted from D_p to S_n.



(j) Mode 7: When load current is completely diverted to S_n, D_p turns off and a process of charging C_{sp} and discharging C_{sn} starts.

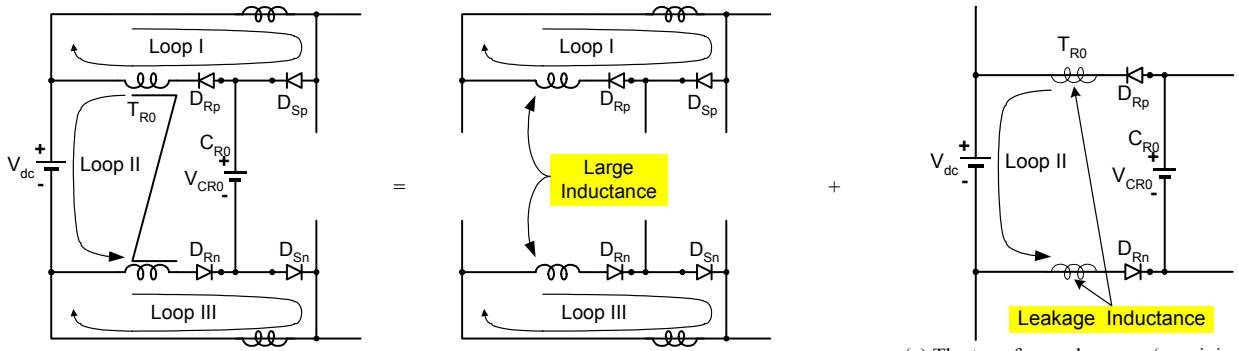


(k) Mode 8: When C_{sn} is fully discharged, the charging current starts to decrease.



(l) Mode 9: The charging current has decreased to zero, and the energy stored in the stray inductance has been transferred to the snubber capacitor.

Fig. 4. Operating modes.



(a) Equivalent circuit of the energy recovery circuit.

(b) The transformer acts as a large inductance to Loops I and III to minimize circulating current.

(c) The transformer has zero (or minimal leakage) inductance toward Loop II to maximize energy recovery current and efficiency.

Fig. 5. Operating principle of the energy recovery circuit.

Mode 5, Fig. 4(g): Because the charging current following through C_{Sp} is bigger than the load current, the surplus is carried by switch S_n. The charging current starts to decrease because V_{Csp} is slightly higher than the dc source voltage, V_{Cs0}. Once the charging current drops below the load current, the operation of the circuit proceeds to Mode 2 and eventually settles at Mode 3.

Mode 0-, Fig. 4(h): Another initial mode in which switch S_p is on but the diode D_p is conducting the load current, i_L. Again, an inductive load is considered and the load current remains constant during the switching process.

Mode 6, Fig. 4(i): S_n is turned on, so a portion of the load current is diverted from D_p to S_n. The current following through S_n increases as the current through the stray inductance and the diode D_p decreases.

Mode 7, Fig. 4(j): When load current is completely diverted to S_n, D_p turns off and a process of charging C_{sp} and discharging C_{sn} starts.

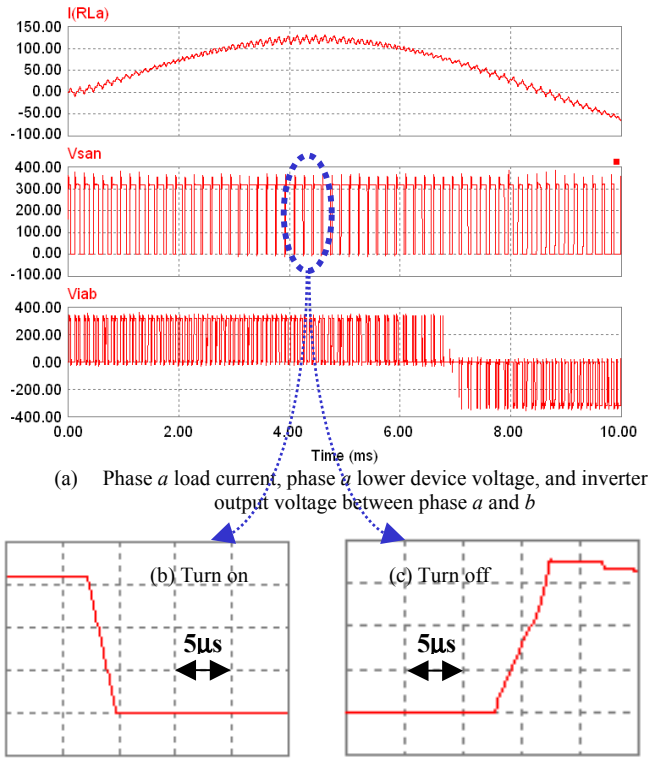
Mode 8, Fig. 4(k): When C_{sn} is fully discharged and clamped at zero voltage, the charging current starts to decrease. During this mode, as the voltage across the capacitor C_{S0} becomes higher than the dc source voltage, the energy recovery circuit starts to transfer energy from the capacitor back to the dc source.

Mode 9, Fig. 4(l): The charging current has dropped to zero, and the energy stored in the stray inductance has been transferred to the snubber capacitor.

Fig. 5 indicates the operating principle of the energy recovery circuit. This circuit has three current loops as illustrated in Fig. 5(a). Loop I includes the stray inductance of the positive dc link, the diodes D_{Sp} and D_{Rp}, and one of the transformer windings. Loop II is the energy recovery path and consists of the diodes D_{Rp} and D_{Rn}, the capacitor C_{R0}, the dc source, and the transformer. Loop III is the negative counterpart of loop I and includes the stray inductance of the negative dc link, the diodes D_{Sn} and D_{Rn}, and the other transformer winding. The transformer is connected like a common mode choke and thus presents a large inductance to Loops I and III, as illustrated in Fig. 5(b), to minimize the loop circulating currents. On the other hand, only the leakage inductance of the transformer is seen in loop II, as indicated in Fig. 5(c), thus maximizing the energy recovery current and efficiency.

III. Simulation and Experimental Results

Fig. 6 shows simulation waveforms of the three-phase PSSS inverter prototype, where I(RLa) is phase *a* load current, Vsan is phase *a* lower device voltage, and Viab is the inverter output voltage between phase *a* and *b*. The snubber circuit parameters are shown in Fig. 2, with the dc voltage V_{dc} = 330 V and stray inductance L_s = 1 µH. The turn-on and turn-off waveforms of Vsan clearly show that dv/dt is reduced and voltage overshoot is clamped at well below 400 V.



(a) Phase *a* load current, phase *a* lower device voltage, and inverter output voltage between phase *a* and *b*

Fig. 6. Simulation waveforms.

Fig. 7 shows a photo of a 150 kVA three-phase PSSS inverter prototype. No dc bus planes were employed, greatly simplifying the dc bus structure. A toroidal magnet was used as the transformer core.

Fig. 8 shows experimental waveforms of the prototype, where Vcep and Vcen are the voltage across the upper and lower switches of a phase leg, respectively, and I_{Rp} and I_{Rn} represent the energy recovery currents in the transformer windings. The turn-off dv/dt is well suppressed at around 300 V/μs, which is much lower than in a hard-switched PWM inverter, whose dv/dt can be easily higher than 3000 V/μs. During each switching, a pulse current on I_{Rp} and I_{Rn} sends snubber energy back to the dc link capacitor, C_{dc}.

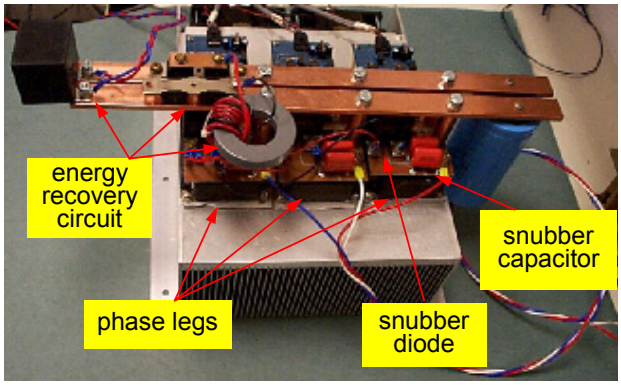


Fig. 7. Photo of a 150 kVA PSSS inverter prototype.

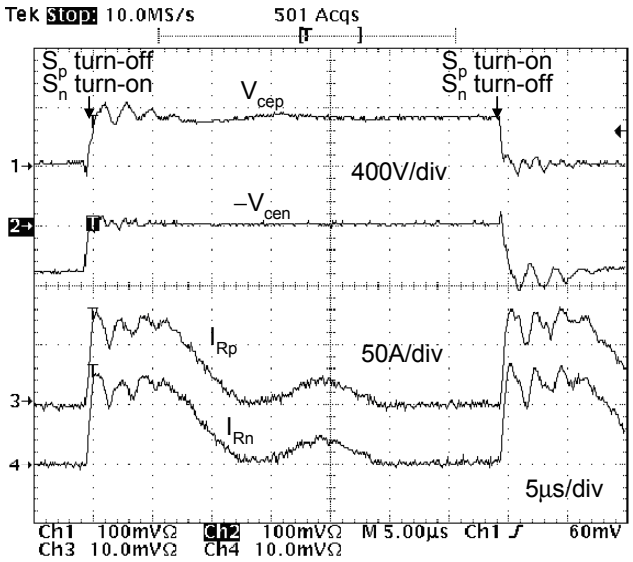


Fig. 8. Experimental waveforms.

IV. PSSS Circuit Design and Considerations

A. Snubber Circuit Design

As discussed in Section II, "PSSS Circuit and Operating Principle" and in Section III, "Simulation and Experimental Results", the dv/dt and di/dt are determined by the snubber capacitance C_S and stray inductance L_s and partially by the load current. The highest dv/dt happens in Modes 4 and 7 when the dc link forms a resonant circuit through the stray inductance and snubber capacitor. For Modes 4 and 7, the upper snubber capacitor voltage V_{Csp} can be expressed as

$$V_{Csp}(t) = V_{Cs0} - \left(V_{Cs0} - V_{Csp}(0)\right)\cos(\omega t) + \frac{I_{Ls}(0)}{\omega C_S}\sin(\omega t) \qquad (2)$$

where V_{Cs0} is almost a constant that equals the dc voltage as shown in Fig. 3, $V_{Csp}(0)$ is the initial voltage of the upper snubber capacitor, $I_{Ls}(0)$ is the initial current through the stray inductor, and $\omega = 1/\sqrt{(2L_s)C_S}$ is the resonant frequency.

The load current affects the initial voltage of the upper capacitor, $V_{Csp}(0)$, and initial current, $I_{Ls}(0)$. The dv/dt from (2) is obtained as

$$\frac{d}{dt}V_{Csp}(t) = \omega\left(V_{Cs0} - V_{Csp}(0)\right)\sin(\omega t) + \frac{I_{Ls}(0)}{C_S}\cos(\omega t). \qquad (3)$$

As can be seen from Eq. (3), if the snubber capacitance is properly designed so that the dv/dt contributed by the initial current is contained, the highest dv/dt occurs at $\omega t = \pi/2$ when the load current is zero, which results in zero initial voltage and current. The highest dv/dt, equal to ωV_{Cs0}, is therefore determined by the resonance frequency of $2L_S$ and C_S, ω. The highest di/dt also occurs in Modes 4 and 7, which can be expressed as

$$\frac{di}{dt} = \frac{V_{Cs0}}{2L_s}. \qquad (4)$$

Therefore, it is obvious that the stray inductance and snubber capacitor are employed to limit both dv/dt and di/dt. Given target numbers for dv/dt and di/dt, snubber capacitance and stray inductance can be determined. The rule of thumb for estimating the stray inductance is 1μH per 1-meter-long conductor.

B. Energy Recovery Circuit Design: Rating and Efficiency

The average power to be recovered through the energy recovery circuit, expressed in Eq. (1), includes two terms. The first term is related to the energy stored in the snubber capacitors, and the second term is related to the energy recovered from the stray inductance over a fundamental cycle. While the latter, denoted as $P_{R(Ls)}$, depends on the load current, I_{Lrms}, and switching sequences, it may be approximated by the following equation for a three-phase inductive load, provided that the switching frequency is higher enough than the fundamental frequency and any switching instance completes before the next one starts so they do not interfere with each other.

$$P_{R(Ls)} \approx 4.31 L_s I_{Lrms}^2 f_{sw}. \qquad (5)$$

Total recovered power for the prototype at a load current of 250 Arms can be calculated by

$$P_R = (6\times 0.1\mu\text{F}\times(400\text{V})^2 + 4.31\times 1\mu\text{H}\times 250^2)\times 10\text{kHz} = 3654\text{W}. \qquad (6)$$

This power has to be recovered through the recovery circuit, comprising the transformer, T_{R0}, and diodes, D_{Rp} and D_{Rn}, back to the dc source. Fig. 8 shows the recovery current waveforms, I_{Rp} and I_{Rn}, at each switching instant. Therefore, the average recovery current is

$$I_{R\_avg} = \frac{P_R}{V_{dc}} = \frac{3654\text{W}}{330\text{V}} = 11\text{A}. \quad (7)$$

The transformer and the diodes can be designed by this average recovery current. Assuming the voltage drop across each diode is V_D and the winding resistance is R_t, the power loss and energy recovery efficiency of the circuit can be approximately expressed as follows:

$$P_{loss} \approx 2I_{R\_avg}^2 R_t + 2V_D I_{R\_avg}, \quad (8)$$

$$\eta = 1 - \frac{P_{loss}}{P_R}. \quad (9)$$

For the prototype, the recovery efficiency is around 97% assuming R_t=0.3 Ω and V_D=1.0 V.

V. Conclusions

The presented PSSS circuit has the following features:

- employing only passive components;
- requiring no additional control;
- allowing any PWM schemes;
- eliminating dc bus plane layout;
- utilizing stray inductance;
- reducing dv/dt and di/dt;
- lowering cost and improving reliability.

The PSSS provides a viable alternative to the existing soft-switching inverters. The PSSS is especially suited for silicon carbide (SiC) device inverters because SiC diodes have no or minimal reverse recovery current, which reduces dv/dt uniformly at both turn-on and turn-off to further soften the switching.

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